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— INVITED PAPER—

InP/GaAsSb/InP Double Heterojunction Bipolar Transistors

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Abstract — InP/GaAsSb/InP double heterojunction bipolar transistors (DHBTs) are some of the fastest bipolar transistors ever fabricated, with current gain cutoff and maximum oscillation frequencies simultaneously exceeding 300 GHz while maintaining breakdown voltages $BV_{CEO} > 6$ V [1]. InP/GaAsSb/InP DHBTs are particularly appealing because excellent device figures of merit are achievable with relatively simple structures involving abrupt junctions and uniform doping levels and compositions. This is a tremendous manufacturability advantage and the reason why some organizations have moved aggressively toward GaAsSb DHBT production despite a relative scarcity of information on the physical properties of the GaAsSb alloy in comparison to GaInAs. The present paper reviews some of the key concepts associated with the use of GaAsSb base layers, and discusses the physical operation InP/GaAsSb/InP DHBTs. In particular, we will describe the implications of the staggered band lineup at the E/B and B/C heterojunctions for charge storage in the devices, and show that InP/GaAsSb/InP DHBTs offer inherent advantages from that point of view. We will also show that GaAsSb-based DHBTs can be expected to display better scalability than GaInAs-based devices because of their inherently superior base Ohmic contacts.

I. Introduction

InP/GaAsSb/InP double heterojunction bipolar transistors (DHBTs) are among the fastest bipolar transistors ever fabricated, with current gain cutoff and maximum oscillation frequencies simultaneously exceeding 300 GHz while maintaining breakdown voltages $BV_{CEO} > 6$ V when implemented with a 2000 Å InP collector [1]. We anticipate that $f_T = 400$ GHz should be achievable with a breakdown voltage of > 4 V in a 1000-1500 Å collector. The staggered band lineup and the absence of collector blocking effect in abrupt junction InP/GaAsSb/InP DHBTs enable a very high current drivability (even with relatively lightly doped emitter layers) that makes these devices attractive for ultrahigh speed digital circuits of the type needed for fiber network and instrumentation applications at 40 Gb/s and beyond. InP/GaAsSb/InP DHBTs feature a very low turn-on voltage $V_{BE,ON} \sim 0.4$ V at $J_C = 1$ A/cm^2 which also makes them attractive for long talk-time wireless applications operating with low battery voltage requirements [2]. InP/GaAsSb/InP DHBTs are particularly appealing because excellent device figures-of-merit are achievable with relatively simple structures involving abrupt junctions and uniform doping levels and compositions: the applicability of these devices outside a

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research laboratory setting has been validated at *Agilent* with the realization of circuit blocks based on conservative device structures: performances are already competitive with published state-of-the-art results for both GaInAs SHBTs and DHBTs [3]. The benefits of simple epitaxial structures allowing superior device performance simply cannot be overstated: InP/GaAsSb/InP DHBTs can be fabricated using selective wet etching techniques, and this is a critical manufacturability advantage when one is faced with the realization of HBTs with sub- 300 Å base layers in a production setting. In addition, C-doped GaAsSb can be grown by MBE and MOCVD, but the MOCVD growth proves extremely advantageous because it can be carried out using H_2 as the carrier gas and organo-metallic sources without running into H-passivation problems like GaInAs does. In this fashion, C- doped GaAsSb layers with hole concentrations as high as 3×10^{20} /cm^3 have been produced at SFU [4]. In general, SIMS analysis indicates that MOCVD-grown C-doped GaAsSb epilayers feature a much lower [H]/[C] concentration ratio than found in GaInAs, a finding of obvious potential interest from a burn-in / reliability point of view.

The situation with InP/GaAsSb/InP DHBTs is in marked contrast to the GaInAs –based DHBT case: the latter require sophisticated grading schemes at both the emitter and the collector (unless an InP emitter is used): by now it is widely understood that even a single extraneous/missing layer in a superlattice grading can have dire consequences on both the device static and dynamic characteristics (such as negative differential conductance, depressed current carrying capabilities, low current gains, large offset and knee voltages, and low cutoff frequencies). *With InP/GaAsSb/InP DHBTs the E/B and B/C junction characteristics are determined by the doping levels, heterojunction band offsets, and the bandgaps, not the effectiveness —or lack thereof— of various grading schemes intended to mask the natural blocking band offset between GaInAs and InP.* In a way, a GaAsSb base affords advantages that are of a similar nature to those provided by HBTs over HEMTs as far as turn-on voltage uniformity goes. Stated differently, InP/GaAsSb/InP DHBTs are practically unaffected if the emitter/collectors layers are off from their nominal design value by ± 50-100 Å.

The increasingly widespread acceptance and independent verification of the aforementioned manufacturing and device performance advantages by various entities of the III-V electronics community is at the root of the fast paced evolution of InP/GaAsSb/InP DHBTs from the status of an apparent technological dead end [5] to a technology worthy of serious consideration today. Industrial initiatives toward the development of GaAsSb –based DHBTs have now been launched in Canada, Europe, Japan and in the United States. A potential outcome of these R&D initiatives is that some organizations may, as we ourselves did at Simon Fraser University, simply abandon the development of GaInAs DHBTs in favor of the better-suited band alignment afforded by the GaAsSb alloy for DHBT applications.

II. Physical Operation of InP/GaAsSb/InP DHBTs

The Emitter/Base Junction

The equilibrium band alignment for an InP/GaAsSb/InP DHBT is shown in Fig. 1: the advantages from a collector blocking point of view are immediately apparent in comparison to the GaInAs-based DHBT case — because the p$^+$ base conduction band edge sits above the InP collector CB edge, electrons are injected into the collector *even under zero electric field conditions* at the B/C heterojunction. Some, perhaps taken aback by the unusual band diagram for a type-II DHBT, have expressed the concern that this approach may displace the "design problem" from the collector to the emitter. Firstly, the emitter is probably a better place to have a

problem in an HBT, if indeed one is going to have to solve one; secondly, there is no "design problem" with an InP emitter on a GaAsSb base as long as the ΔE_C is not too sizable. In fact, for a lattice-matched GaAs$_{0.51}$Sb$_{0.49}$ base with $\Delta E_C \sim 0.15$ eV at room temperature [6], a little bit of reflection should suffice to convince one that electrons experience thermal injection from the InP emitter into the GaAsSb base when the junction is forward biased. Back injection of holes is simply a non-issue because of the very large valence band discontinuity of $\Delta E_C \sim 0.78$ eV. This band lineup enables a very simple emitter structure consisting of a GaInAs contact layer followed by an abrupt junction to the InP emitter *per se*. On the other hand, one can also opt for a type-I Al$_{0.48}$In$_{0.52}$As emitter that would launch electrons into the GaAsSb base with roughly some 0.1 eV of kinetic energy, based on our measurement of the band alignment between InP and GaAs$_{0.51}$Sb$_{0.49}$ [6], and on transitivity arguments with AlInAs. Care probably needs to be used in launching 'hot' electrons in GaAsSb because the ternary alloy may well have a low intervalley separation since both its binary constituents feature low Γ-L valley separations (GaAs: 0.29 eV and GaSb: 0.08 eV). Thus, even if feasible, hot electron injection beyond ~ 0.1 eV with an Al-rich Al$_{0.48+x}$In$_{0.52-x}$As emitter is probably not a very good idea as far as speeding up transport across base is concerned.

Once across the E/B junction and into the quasi-neutral GaAsSb base, minority carrier electrons diffuse toward the collector with an apparent mobility of 900-1000 cm^2/Vs according to our most recent estimates. Others [7] believe the electron mobility in the base could be closer to values reported for GaInAs, and a definitive measurement remains to be carried out. This notwithstanding, the possibility of grading the base exists if it ever becomes necessary, although in our opinion it takes away from the simplicity of implementation inherent with InP/GaAsSb transistors. With an AlInAs emitter, nearly $4kT$ become available for grading across the base: apparently the most favorable grading approach would involve the formation of a Ga-rich (Al,Ga)AsSb base layer because the GaAsSb alloy features a stronger bandgap bowing than GaInAs, and that would diminish the potential impact of a group-V grading across the base.

The Base/Collector Junction

The staggered band lineup at GaAsSb/InP heterojunctions reduces the collector design problem to a consideration of doping and thickness of the InP collector for a given peak f_T current density J_C because electrons can be injected across the heterojunction *even under flat band conditions (i.e at high current density) at the B/C junction*. B/C grading design is not necessary, as the alloy potential effect[1] first described by Tiwari is non-existent in this system [8]. A simple uniformly doped InP collector of thickness W_C can thus be used with an abrupt heterojunction to the GaAsSb base. The resulting InP/GaAsSb/InP DHBT structure is thus nearly symmetric and about as simple as any transistor structure is going to get. Besides its simplicity, the GaAsSb base is directly sandwiched by (relatively) high thermal conductivity InP on both sides.

It has long been known that type-I GaInAs-based DHBTs with attractive device performances *can* be achieved [9], but it is interesting to consider the issues involved in such an undertaking: *a)* the blocking

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[1] The alloy potential effect occurs when the increasing energy gap at a graded B/C junction is revealed as a result of the traveling electron space charge. Careful junction design and implementation is required to manage the effect by tailoring the electric field profile at the junction. Eventually, for a high enough current density, a retarding quasi-electric field appears at the junction that reduces the electron exit velocity from the base and cuts down the transistor cutoff frequency.

potential of 0.25 eV between GaInAs and InP results in a retarding quasi-electric field of $125/t$ kV/cm if a $200t$ Å grading length is used, and this sizable quasi-electric field intensity must be compensated by a combination of doping profile and applied junction reverse bias V_{CB}; b) the extent to which grading layers affect the electron velocity profile through the collector region; and c) the extent to which potential base dopant (Be/Zn, but not C) out-diffusion will interfere with the intended B/C band profile. Obviously, all these design issues can be addressed by a combination of less than mature numerical modeling tools and brute force trial-and-error.

In principle, based on the reported band alignment, electron injection from a GaAsSb base into an InP collector occurs by "ballistically" launching electrons with roughly $\Delta E_C = 0.15$ eV initial kinetic energy [5]. In practice things may occur somewhat differently: band gap narrowing due to the high doping concentrations of $4\text{-}8 \times 10^{19}$ /cm^3 used in GaAsSb bases may reduce ΔE_C below 0.15 eV, just as will the use of an As rich alloy in the base layer. A non-zero launching energy is expected to be beneficial from a collector signal delay time point of view because high velocities can be achieved over significant distances and over a range of electric fields in InP. Brennan and Hess considered the effects of launching energy in InP and reported that $E_i = 0.1$ eV would result in a velocity of $5.5\text{-}6.0 \times 10^7$ cm/s maintained over nearly 1500 Å in a field of 10 kV/cm. By contrast, $E_i = 0.42$ eV would lead to $\sim 8.5 \times 10^7$ cm/s maintained over nearly 1000 Å [10].

The staggered band lineup in InP/GaAsSb/InP DHBTs has interesting consequences inasmuch as charge storage is concerned during transistor operation. We previously contrasted the behavior of GaInAs SHBTs and DHBTs to that of GaAsSb based devices and found that the GaInAs DHBT features a dramatic increase of charge storage at high current densities because of the alloy potential effect at the B/C junction results in a sharp increase of the minority electron stored in the base layer. The InP/GaAsSb/InP DHBT features an altogether different behavior which was first discovered by Tom MacElwee of *Nortel Networks* while measuring devices fabricated at the SFU-CSDL (see Fig. 2): C_{BE} first dips with increasing current density and reaches a minimum value corresponding to the peak f_T bias occurring for the condition of zero electric field at the B/C junction. Further increases in current density reverse the electric field at the B/C junction resulting in the formation of a small field-induced thermionic electron barrier at the B/C junction. Despite the smallness of the induced barrier E_B, it is seen to have a tremendous effect on the base charge storage because it can be expected to reduce the effective base exit velocity by a factor $\sim\exp(-E_B/kT)$, resulting in a sharp rise in C_{BE} and a drop in $f_T(J_C)$. An indication of the smallness of E_B is confirmed by measurements of $f_T(J_C)$ characteristics as a function of temperature: as Fig. 3 clearly shows, the f_T roll-off with increasing current at higher temperatures becomes less abrupt as the chuck temperature increases because more base electrons can thermally overcome the small field-induced barrier at the B/C junction. Fig. 3 also shows that the current for peak f_T decreases with increasing chuck temperature as a result of the decreasing electron velocity in the InP collector at higher temperatures.

It is interesting to reflect on the implications of the above findings: we have found that InP/GaAsSb/InP DHBTs reach peak performance for zero B/C electric fields. In contrast, GaInAs –based DHBTs rely on a high B/C electric field to overcome the alloy potential due to the increasing energy gap moving from the base toward the collector, and this is true whether a bandgap grade or a launcher structure is used. This observation suggests that InP/GaAsSb/InP DHBTs would perform well even under low B/C biases V_{CB} such as those encountered in some bipolar logic families such as current mode logic (CML) circuits. Indeed, Fig. 4 shows that devices

maintain excellent cutoff frequencies even in saturation mode. This is because the large $\Delta E_V = 0.78$ eV at the GaAsSb/InP B/C heterojunction completely suppresses hole injection from the base into the collector.[2]

III. Scalability Issues

Antimonides generally feature a low hole Schottky barrier height which enables the formation of very low resistance p-type Ohmic contacts, an advantage that is in principle compounded by the affinity of GaAsSb layers for C-doping to very high levels. We have measured TLM base contact specific resistances for non-alloyed contacts as low as 10^{-7} Ohms-cm^2, a value for which the contact transfer length becomes comparable in magnitude to the error on the TLM gap spacing measurement in a scanning electron microscope (~ 0.1 μm). Roughly speaking, we have found that Ohmic contacts on GaAsSb bases typically yield 5-10× better Ohmics than on GaInAs, and this finding has been confirmed by others as well. This bodes very well for ultra-scaled DHBTs with deep submicron emitters since for such devices the base resistance no longer is dominated by the base spreading resistance (as it is with 1-2 μm wide emitters) but rather by the base metal/semiconductor contact itself.

We estimate that the hole Schottky barrier on GaAsSb should be of the order of 0.27 eV (compared to roughly 0.45 eV for metals on GaInAs). Based on these values, Fig. 5 shows the calculated specific contact resistance as a function of the base doping level: the plot shows that GaAsSb is expected to maintain an advantage up to $\sim 10^{20}$ /cm^3. The different slopes in Fig. 5 is due to the difference in the valence band density of states for GaInAs and GaAsSb. Fig. 6 shows the evolution of f_{MAX} as a function of emitter width for a 250 GHz InP/GaAsSb/InP DHBT and shows that even conservatively scaled triple mesa devices maximum oscillation frequencies that are very close to what a GaAsSb transferred substrate device would show. Fig. 6 also shows the impact of a 10× degradation in base contact resistance (which is a typical contact resistance for GaInAs devices). Obviously, the excellent base Ohmic contact allows the device to scale very well.

Acknowledgements

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[2] A side benefit of the large ΔE_V is that the hole injection into the collector through base pushout that occurs in SHBTs (and in some launcher-type DHBTs with a narrow gap collector section) at high current levels does not occur in GaAsSb DHBTs. The GaAsSb DHBTs are therefore not subject to the resonant enhancement of Mason's unilateral power gain U that can result in grossly overestimated values of f_{MAX} when U is extrapolated at -20 dB/dec from a frequency domain where U is resonantly enhanced by the injection of holes into the collector region. Bosse Willén and Heinz Jäckel from KTH/Stockholm and ETH/Zurich have pointed out this mechanism and investigated its impact on the perceived device performance [11]. They have shown that following a resonance U can roll off as fast as -40 dB/dec. Clearly, if the last measurement frequencies overlap with the frequency band of resonant enhancement, the f_{MAX} value obtained through -20 dB/dec extrapolation is of little relevance.

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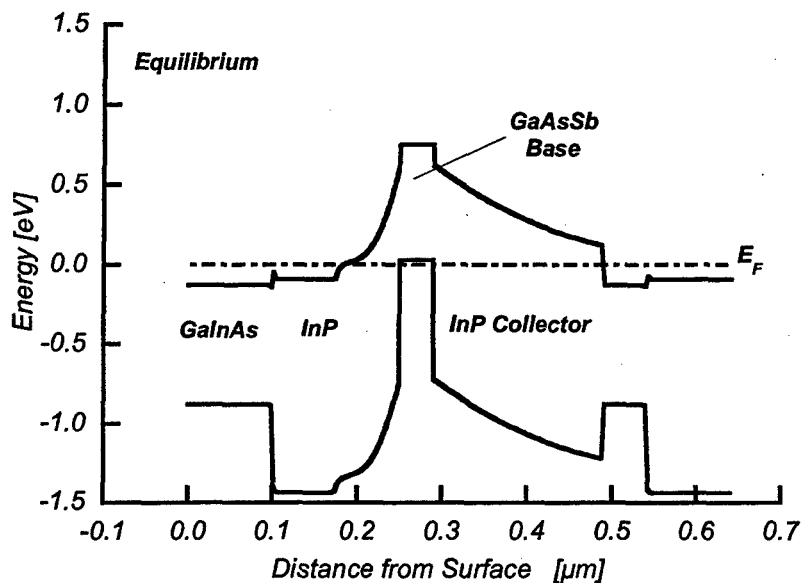
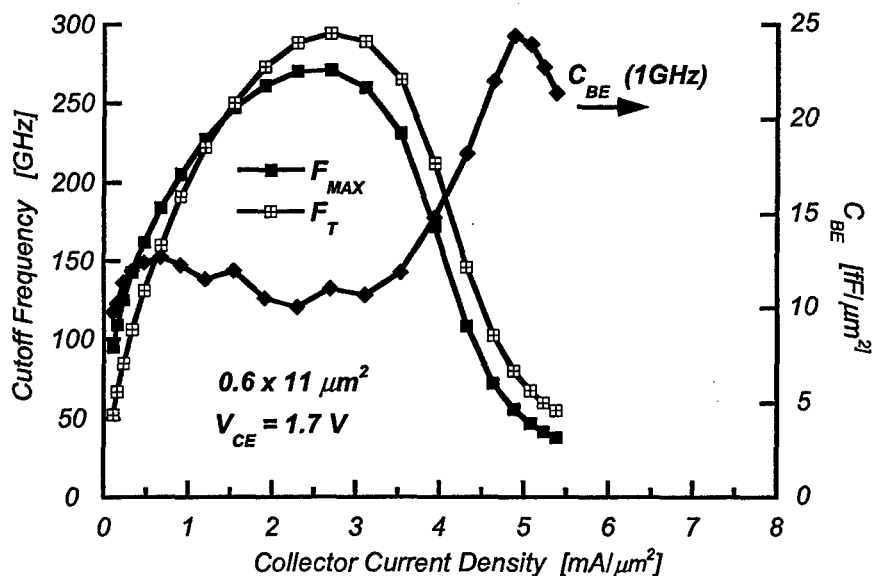Figure 1: Equilibrium band diagram for an InP/GaAsSb/InP DHBT.

Figure 2: f_T and f_{MAX} plotted as a function of collector current density for an InP/GaAsSb/InP DHBT with a 200 Å base and a 2000 Å InP collector. C_{BE} displays an interesting behavior that is markedly different from the increases seen in type-I GaInAs or GaAs based SHBTs and DHBTs. For InP/GaAsSb devices, f_T peaks when the electric field drops to zero at the B/C junction, and further increases in J_C induce a small electrostatic barrier at the B/C that dramatically increases charge storage above 4 mA/µm² in this case. Measurement by T. MacElwee, *Nortel*.
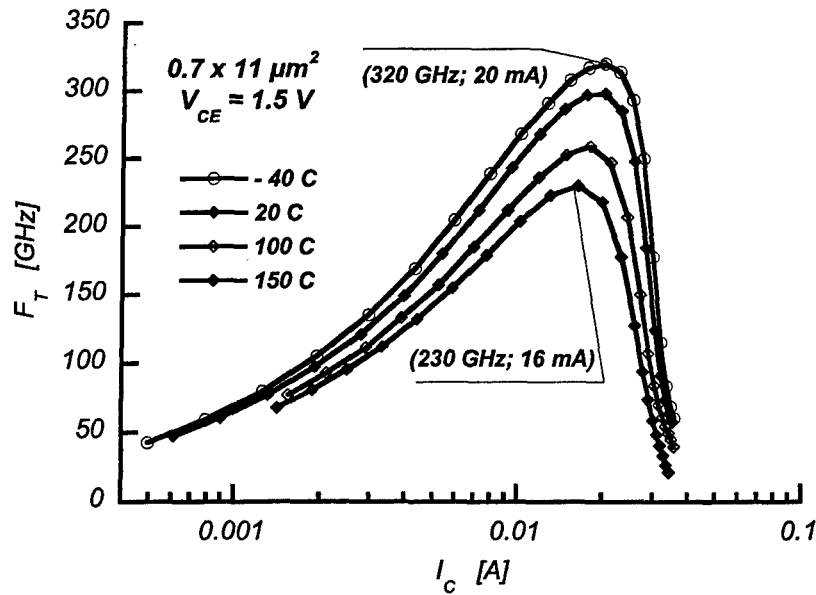
Figure 3: f_T dependence on temperature between –40 C and +150 C chuck temperature. Note that the high current roll off is less abrupt at higher temperatures, indicating that the electrostatic barrier at the B/C junction is small. The peak f_T current decreases with increasing temperature as a result of the lower electron velocity in the InP collector. Data by T. MacElwee, *Nortel*.
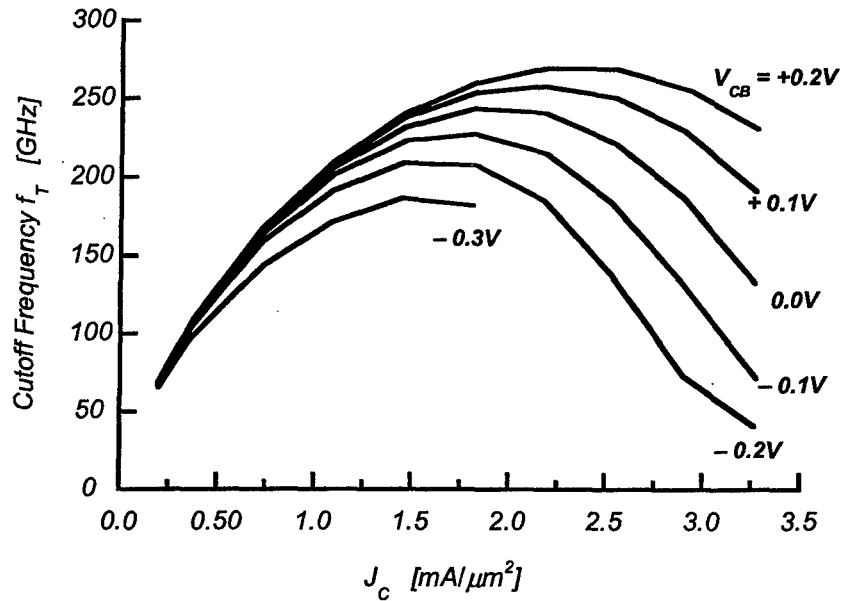

Figure 4: f_T dependence of a 200 Å base InP/GaAsSb/InP DHBT with a 2000 Å InP collector. The device clearly maintains excellent dynamic properties even in saturation mode. The data suggest that GaAsSb-based DHBTs should perform very well in ultrahigh speed CML circuits.
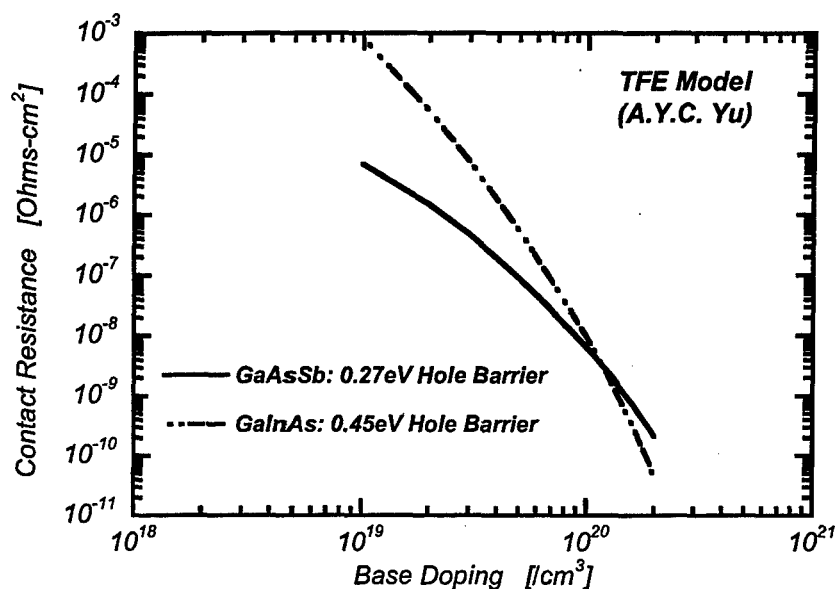
Figure 5: Calculated dependence of base specific contact resistance on base doping for GaAsSb and GaInAs base layers. The cross-over at very high doping levels occurs because the calculation assumes a lower valence band density of states for GaInAs —this assumption may no longer be valid for extremely high doping densities.
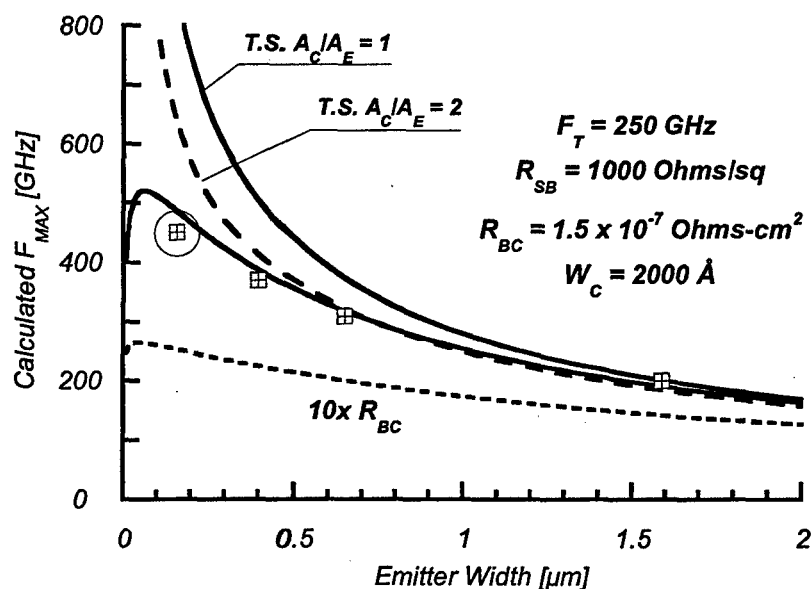

Figure 6: Calculated f_{MAX} for triple mesa InP/GaAsSb/InP DHBTs assuming a 0.5 μm base contacts. The two upper curves represent GaAsSb transferred substrate devices with the indicated area ratios, and the lower dashed curve shows the effect of a tenfold increase in contact resistance on the performance of mesa devices.